# Does Coupling Affect the Security of Masked Implementations?

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Svetla Nikova
Vincent Rijmen

13/04 – COSADE 2017 – Paris

Does coupling
affect the security of
masked implementations ?

# It Might…

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The influence from coupling is observable

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but pinpointing exact source is hard

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and many open questions remain.

# Does coupling affect the security of masked implementations?

**Masking**

What can go wrong?

Sources of coupling

Detecting coupling in practice

Implications

# Masking is a countermeasure against side-channel analysis

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$Z$

Sensitive Value

# Masking is a countermeasure against side-channel analysis

$$\underbrace{Z}_{\text{Sensitive Value}} \oplus \overbrace{M_1}^{\text{Random Number}}$$

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Random Number

$$Z_{masked} = Z \oplus M_1$$

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Masking Scheme

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Masking Scheme

- How to share a sensitive value

- How to compute on the shares

- Assumptions on the device’s leakage behavior

# Wrong assumptions can violate the side-channel resistance

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$((Z \oplus M_1) \oplus M_2) \oplus M_1 = Z \oplus M_2$ Mask refreshing

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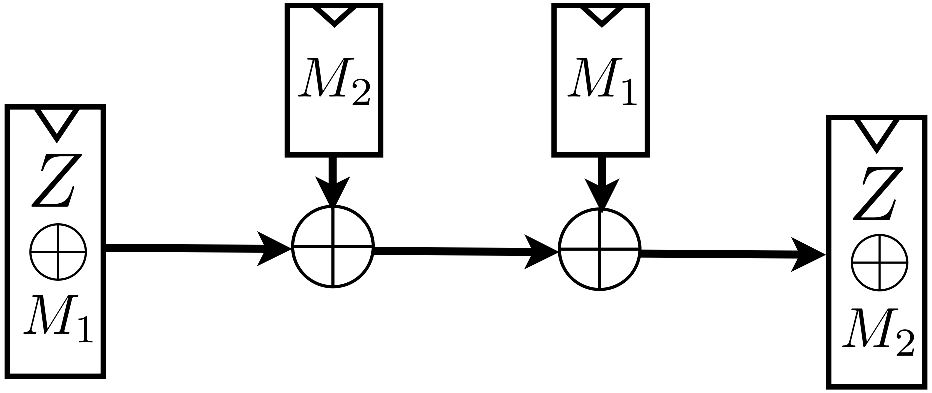
Mask refreshing



Violated assumption

Delay on $M_2$ unmasks Z

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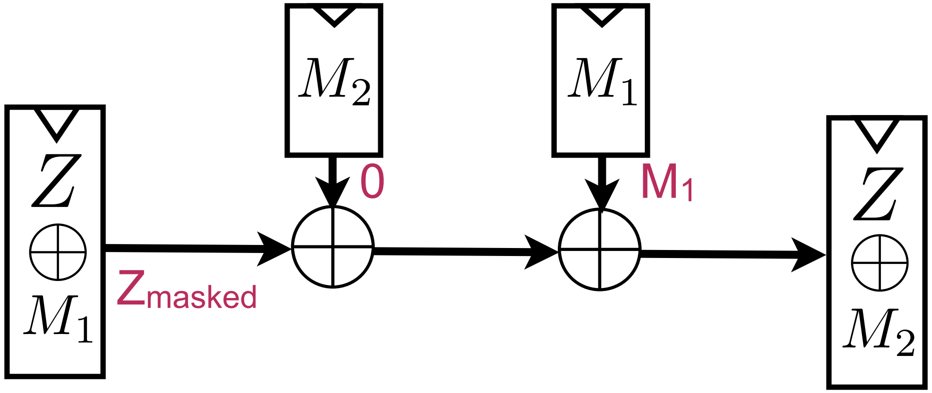

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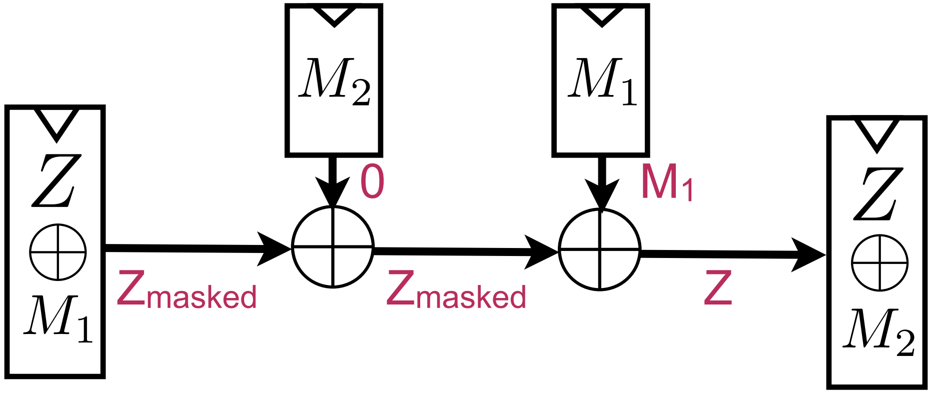
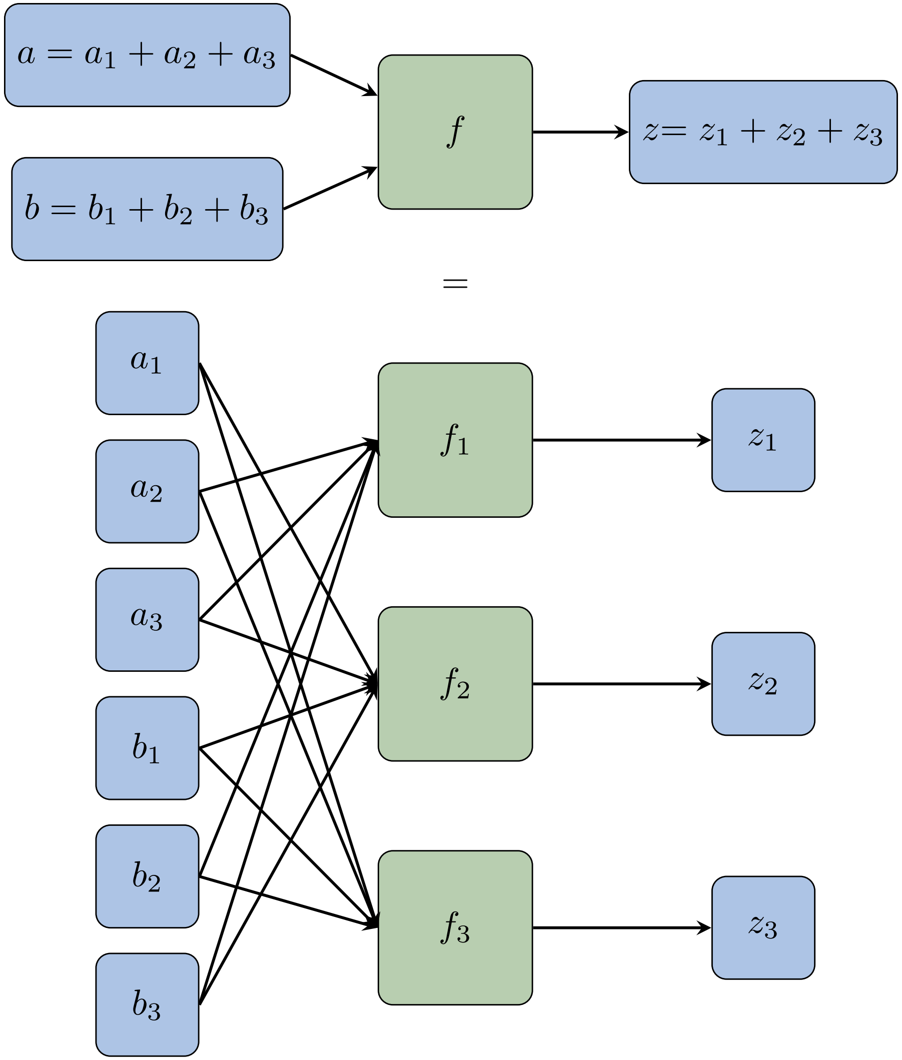


Violated assumption

Delay on $M_2$ unmasks Z

Early propagation and glitches deteriorate the effect of masking

# Threshold implementations are secure in the presence of glitches



Minimal assumptions on the underlying hardware

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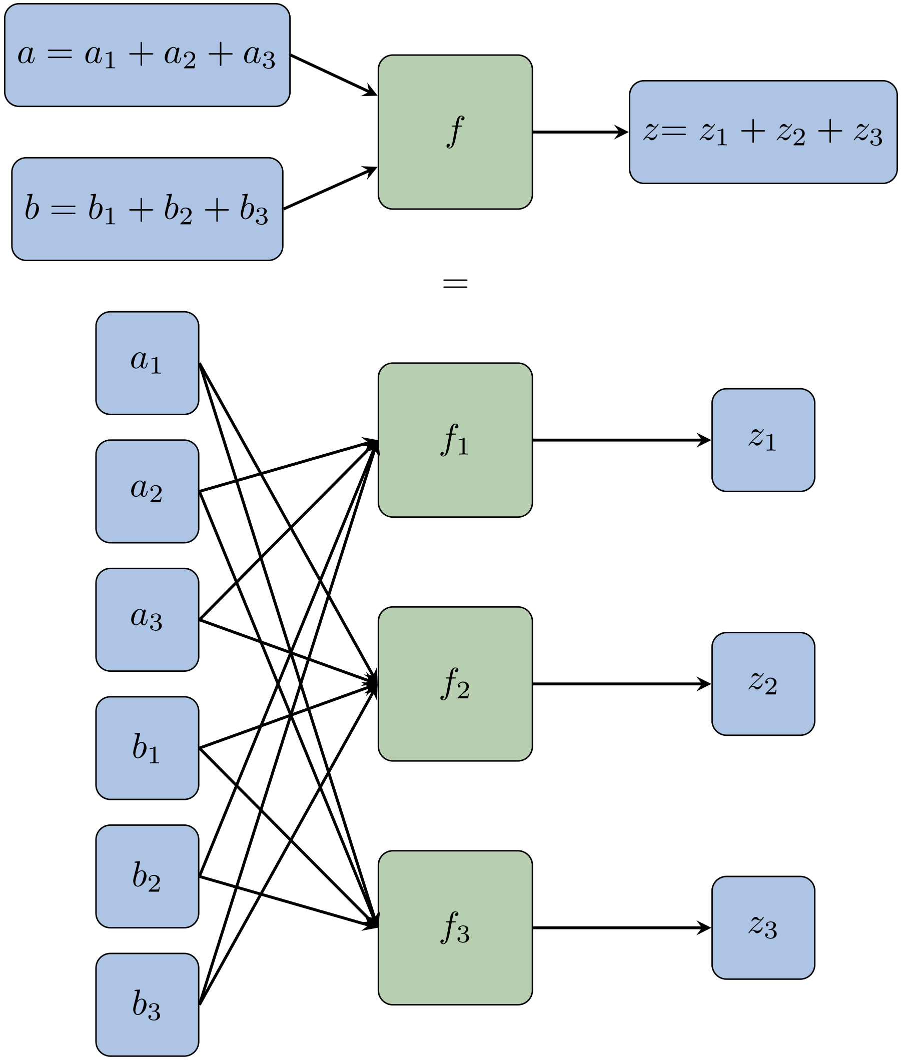

Minimal assumptions on the underlying hardware

Non-completeness of component functions against leakage from glitches

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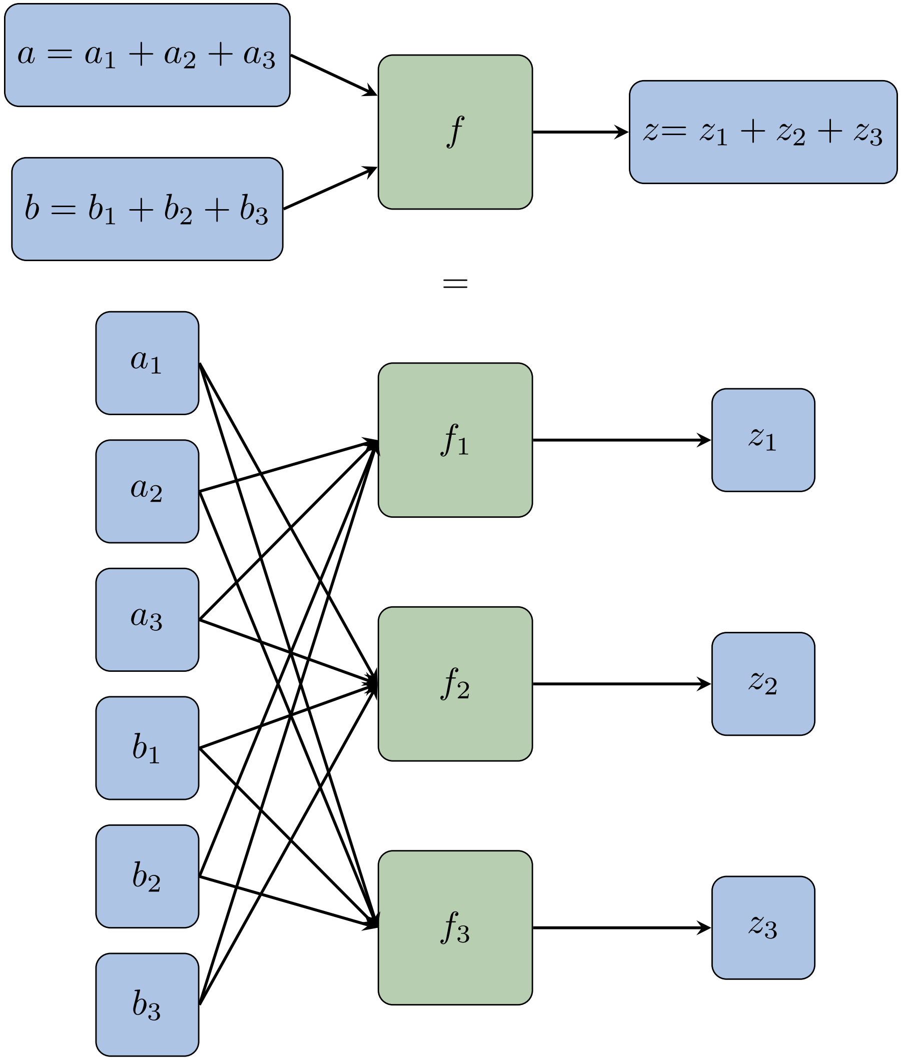
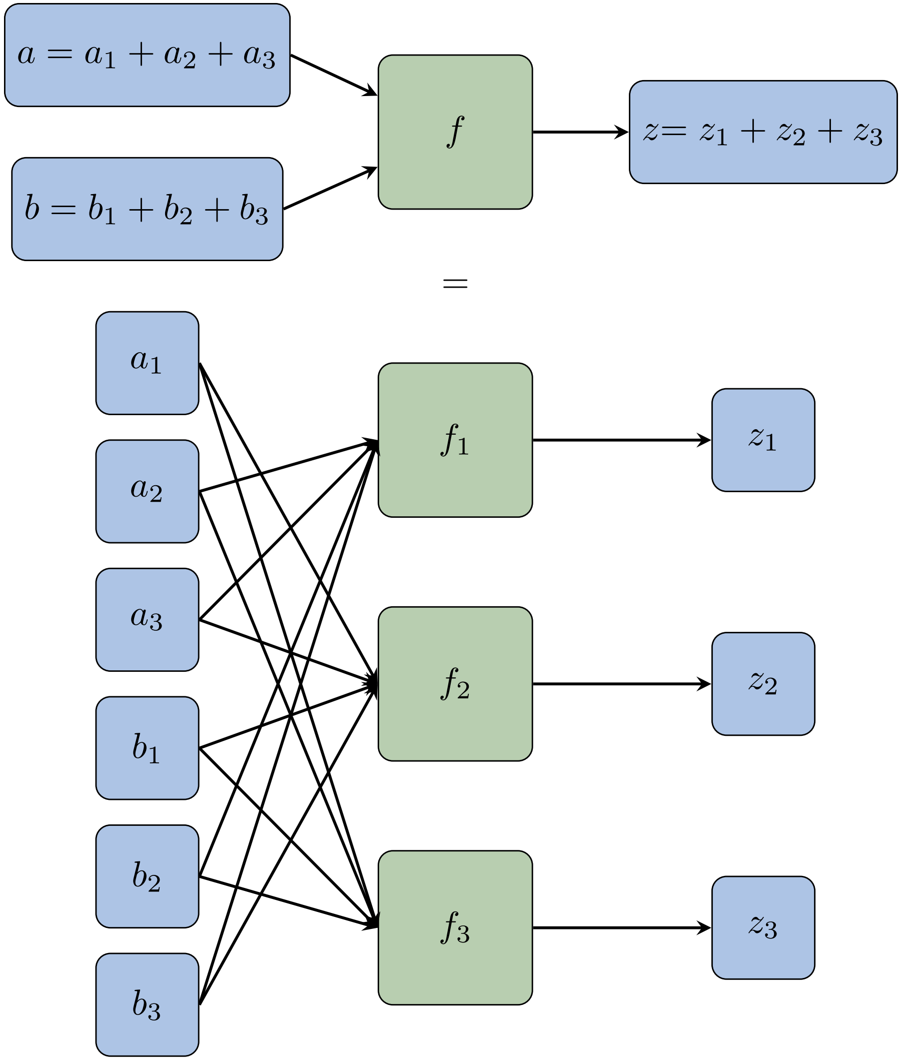


Minimal assumptions on the underlying hardware

Non-completeness of component functions against leakage from glitches

Leakage of the different shares need to be **independent**

# TI assumes the shares to leak independently



If one component function influences another, non-completeness is broken

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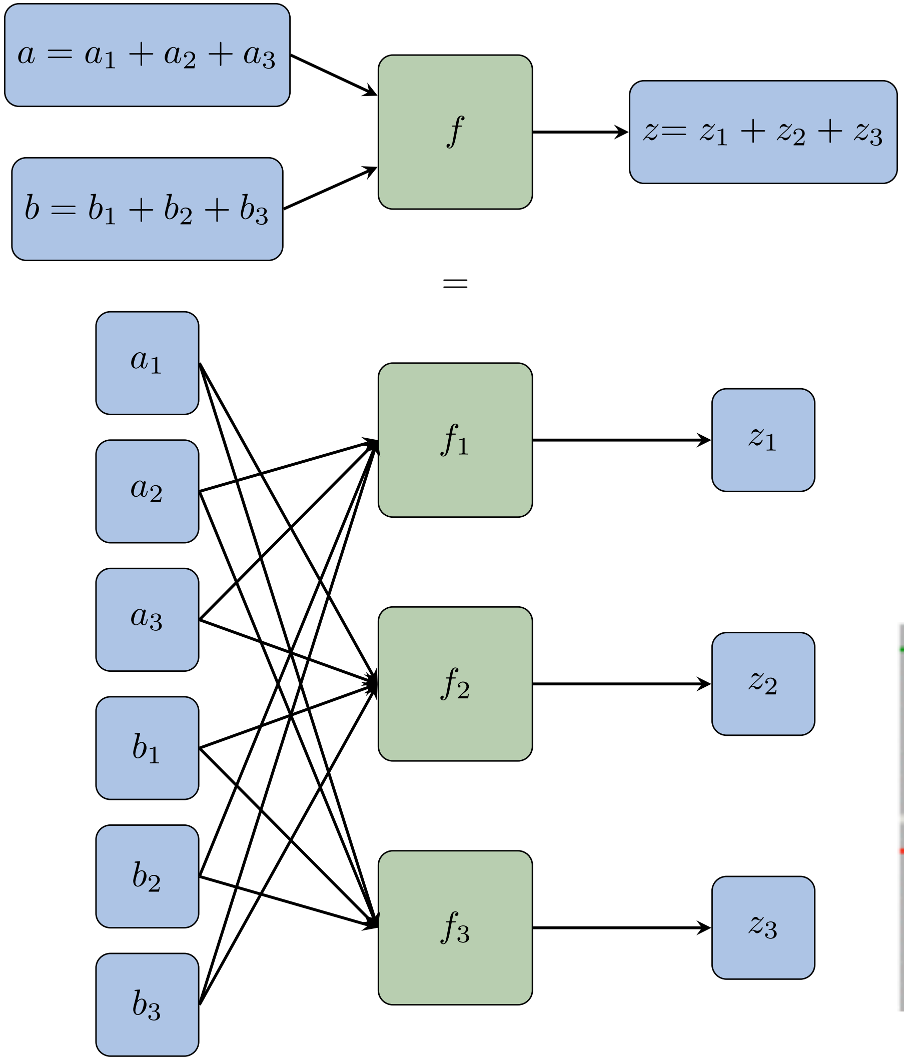

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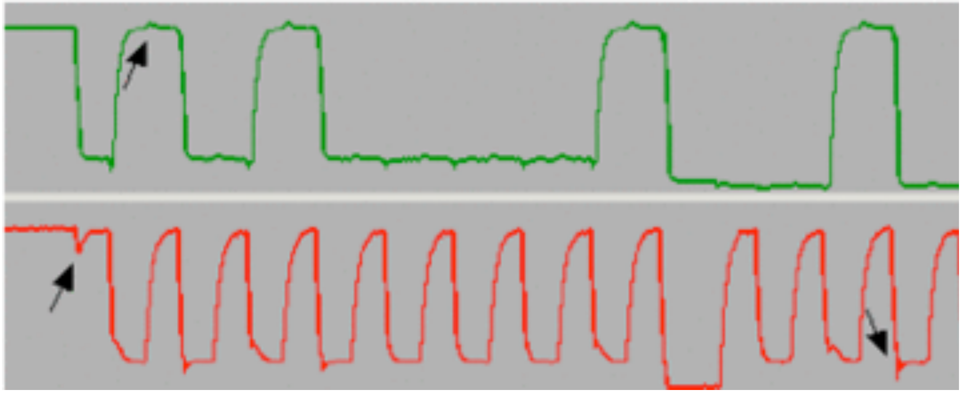


# Does coupling affect the security of masked implementations?

Masking
  What can go wrong?

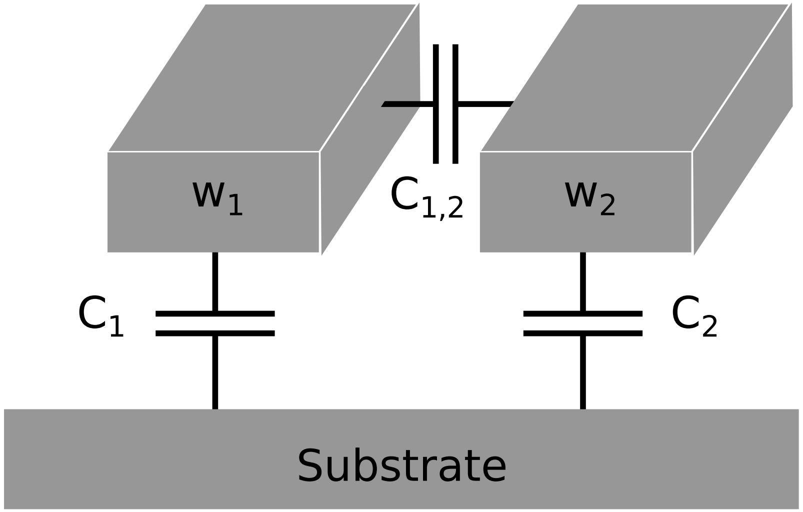
**Sources of coupling**
  Proximity of shares

Detecting coupling in practice

Implications

# Crosstalk couples different shares

L(x1, x2) L(x2, x3)



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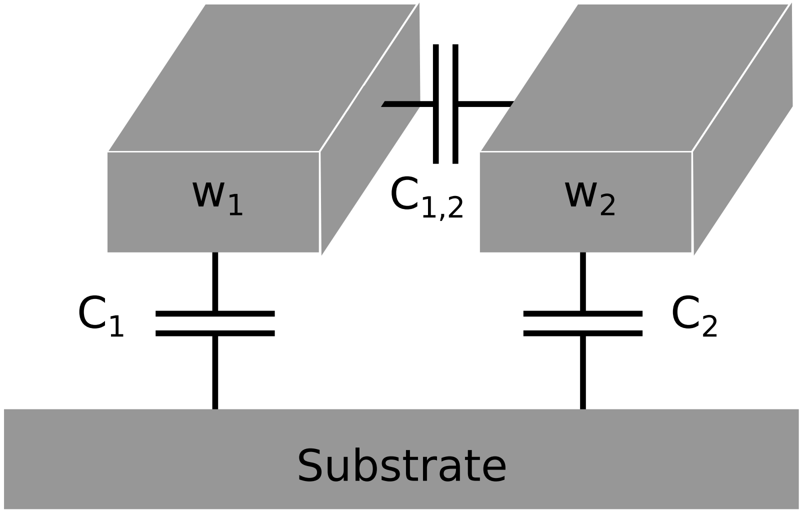
L(x1, x2)   L(x2, x3) → When coupled: L(x1, x2, x3)



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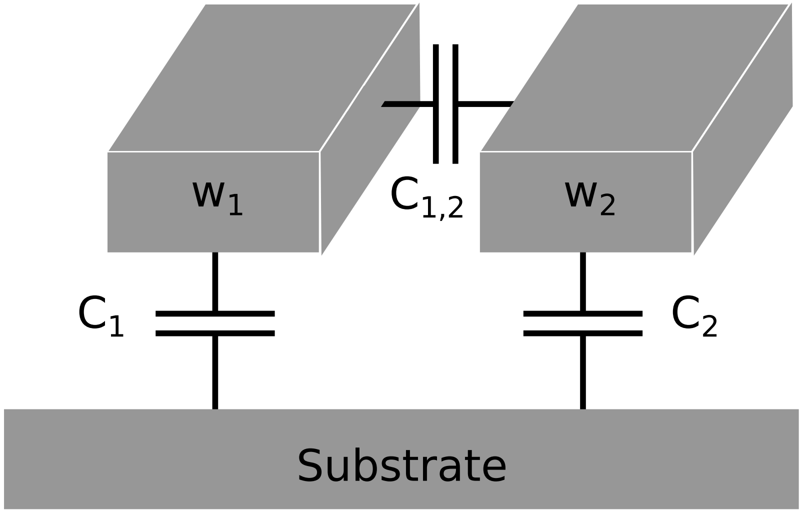


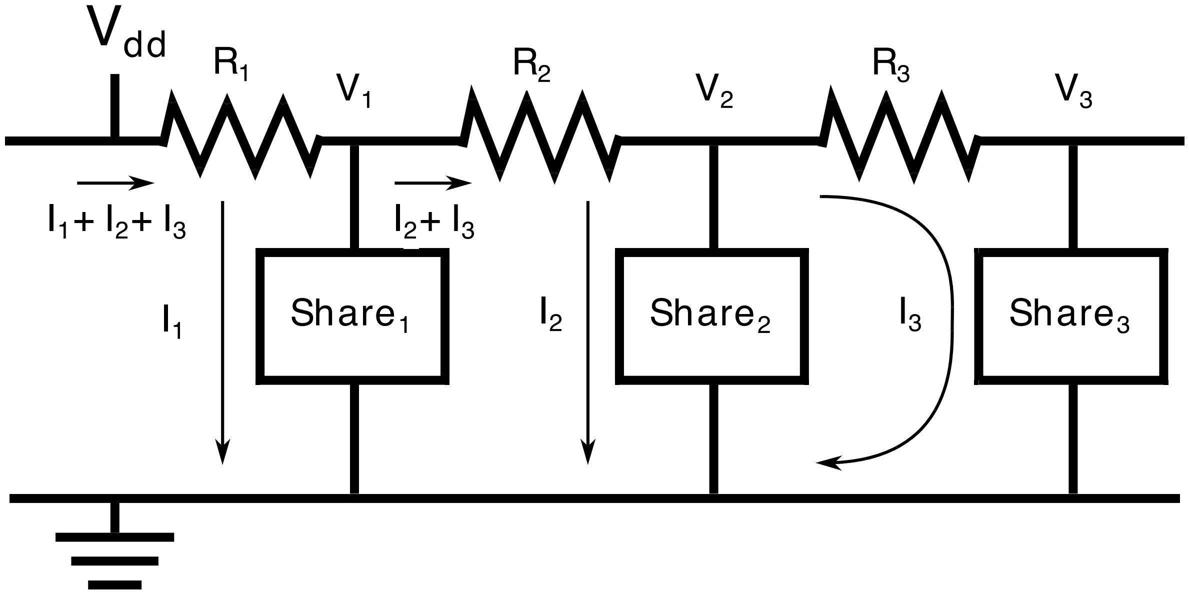
$$C = \frac{e_R \quad e_0 \quad A}{d}$$

A is area

d is **proximity**

# IR Drop couples different shares

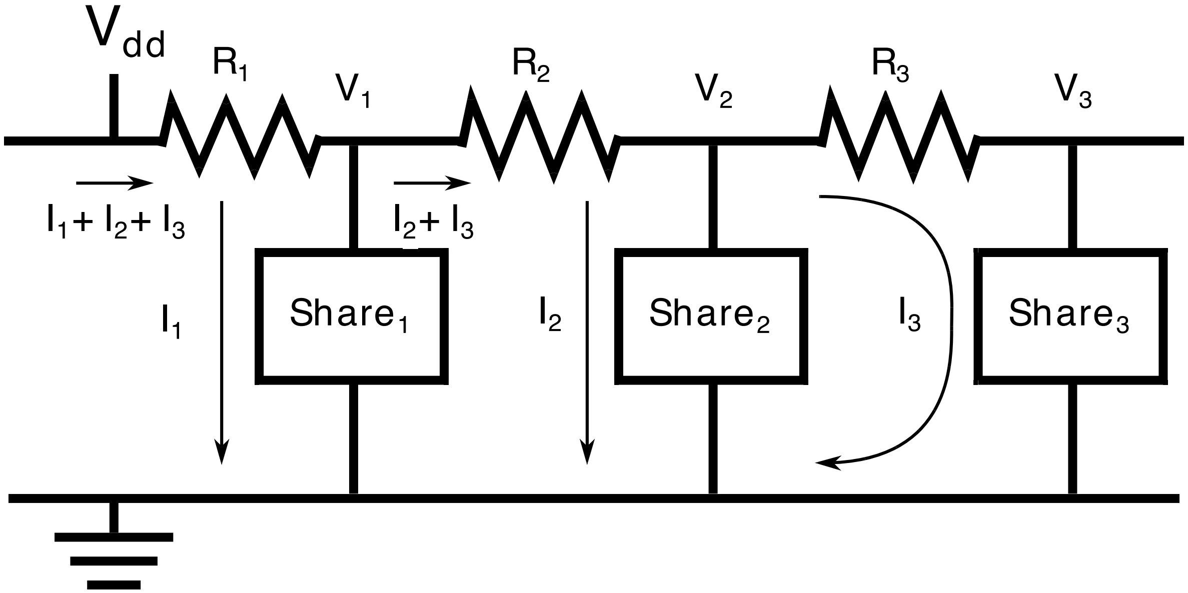
Power and ground distribution
have finite conductance



# IR Drop couples different shares

Power and ground distribution have finite conductance

$$V_1 = V_{dd} - (I_1 + I_2 + I_3)R_1$$
$$V_2 = V_{dd} - (I_1 + I_2 + I_3)R_1 - (I_2 + I_3)R_2$$
$$V_3 = V_{dd} - (I_1 + I_2 + I_3)R_1 - (I_2 + I_3)R_2 - I_3R_3\,.$$



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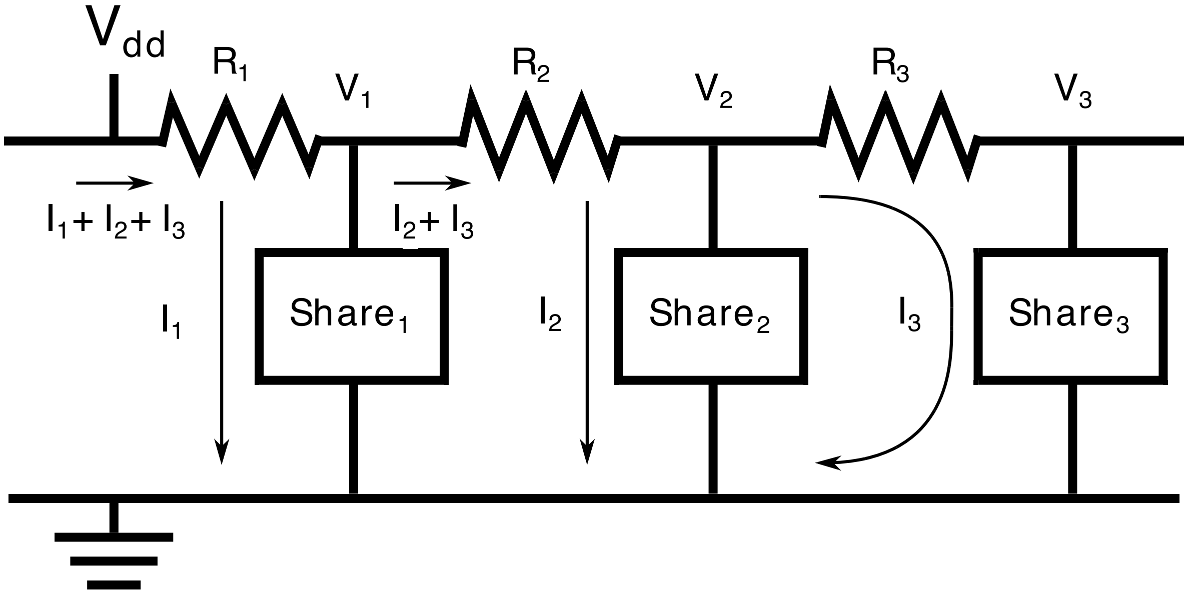

$$P_{inst,Share1} = I_1 V_1 = V_{dd} I_1 - I_1^2 R_1 - I_1 I_2 R_1 - I_1 I_3 R_1$$
$$P_{inst,Share2} = I_2 V_2 = V_{dd} I_2 - I_1 I_2 R_1 - I_2^2 R_1 - I_2 I_3 R_1 - I_2^2 R_2 - I_2 I_3 R_2$$
$$P_{inst,Share3} = I_3 V_3 = V_{dd} I_3 - I_1 I_3 R_1 - I_2 I_3 R_1 - I_3^2 R_1 - I_2 I_3 R_2 - I_3^2 R_2 - I_3^2 R_3 \,.$$

# IR Drop couples different shares

Power and ground distribution have finite conductance

$$V_1 = V_{dd} - (I_1 + I_2 + I_3)R_1$$
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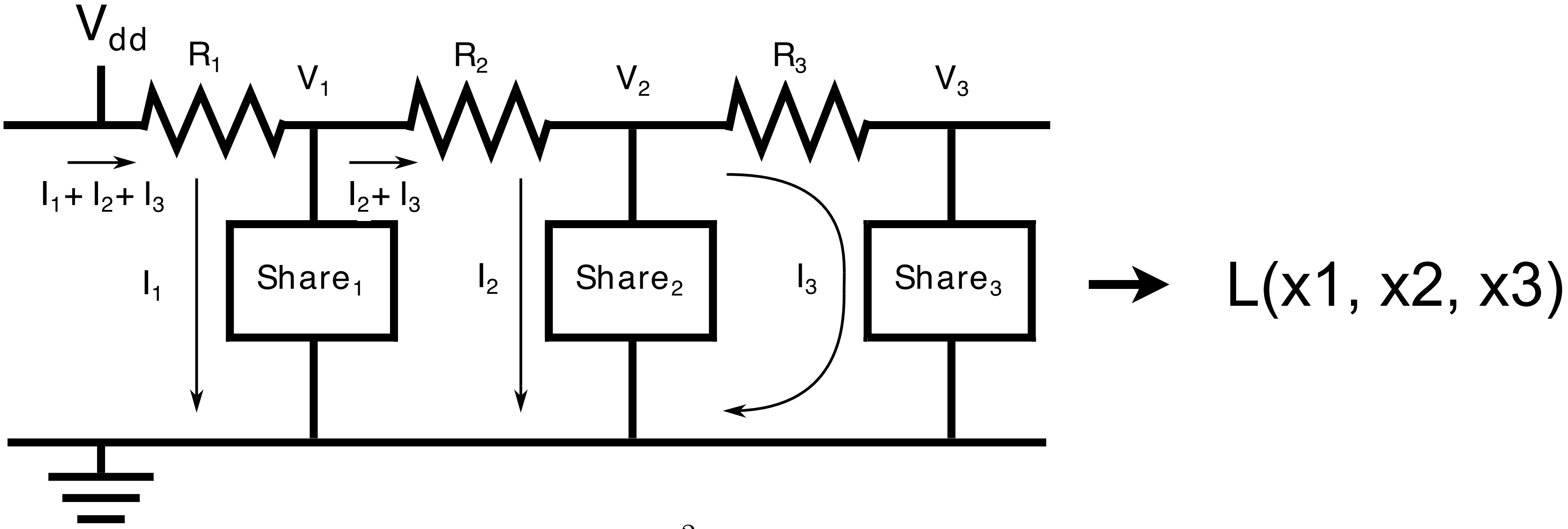

$$P_{inst,Share1} = I_1V_1 = V_{dd}I_1 - I_1^2R_1 - I_1I_2R_1 - I_1I_3R_1$$
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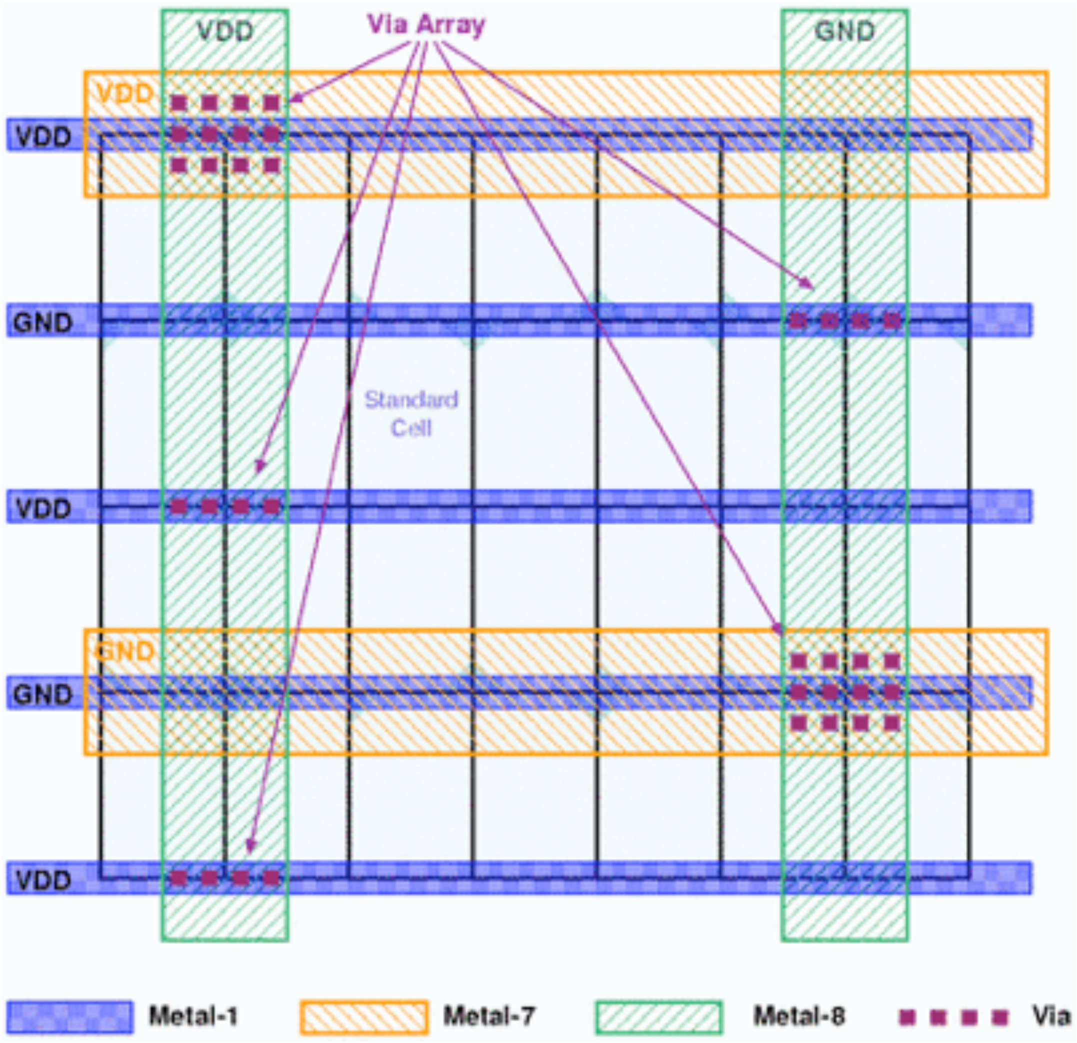
$$P_{inst,Share3} = I_3V_3 = V_{dd}I_3 - I_1I_3R_1 - I_2I_3R_1 - I_3^2R_1 - I_2I_3R_2 - I_3^2R_2 - I_3^2R_3\,.$$

# Proximity leads again to coupling



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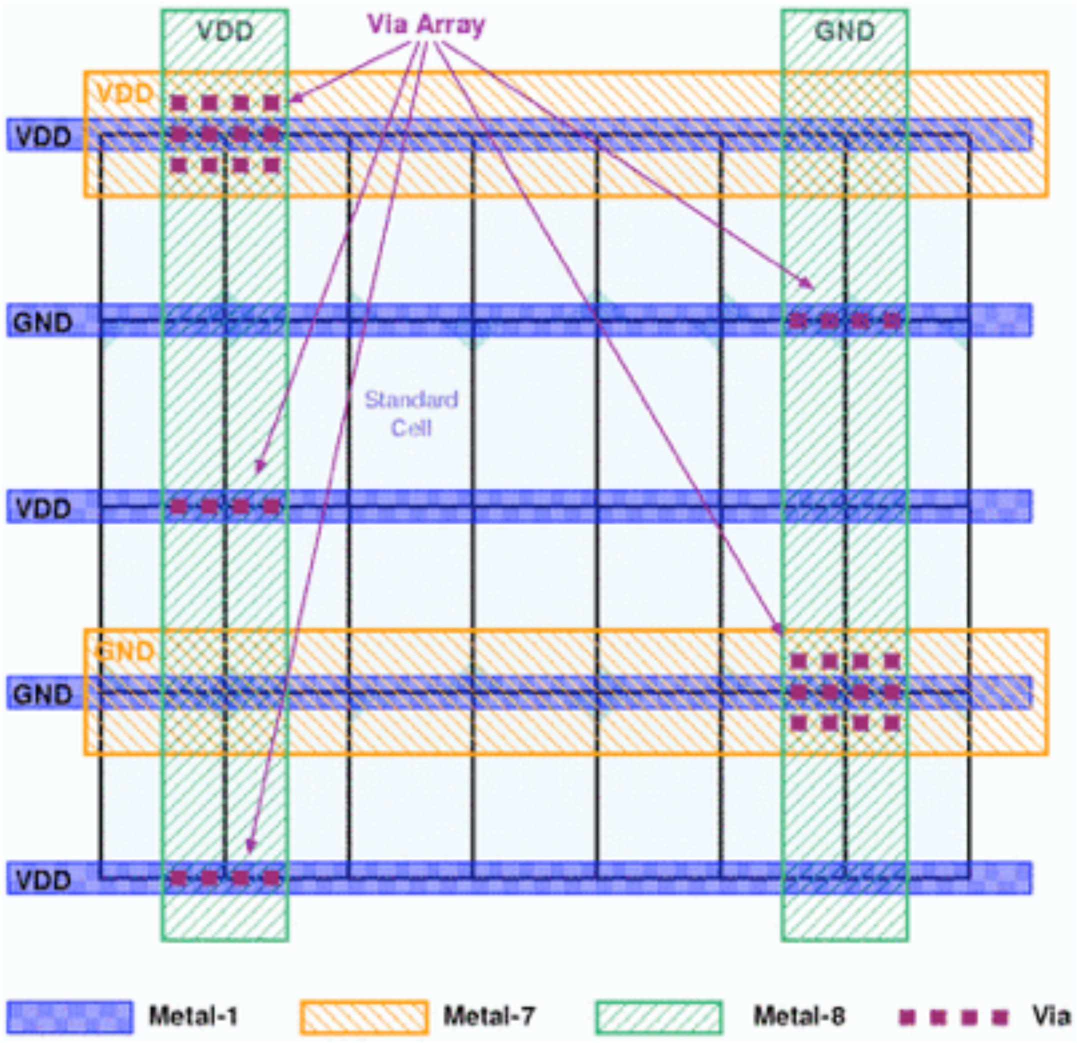
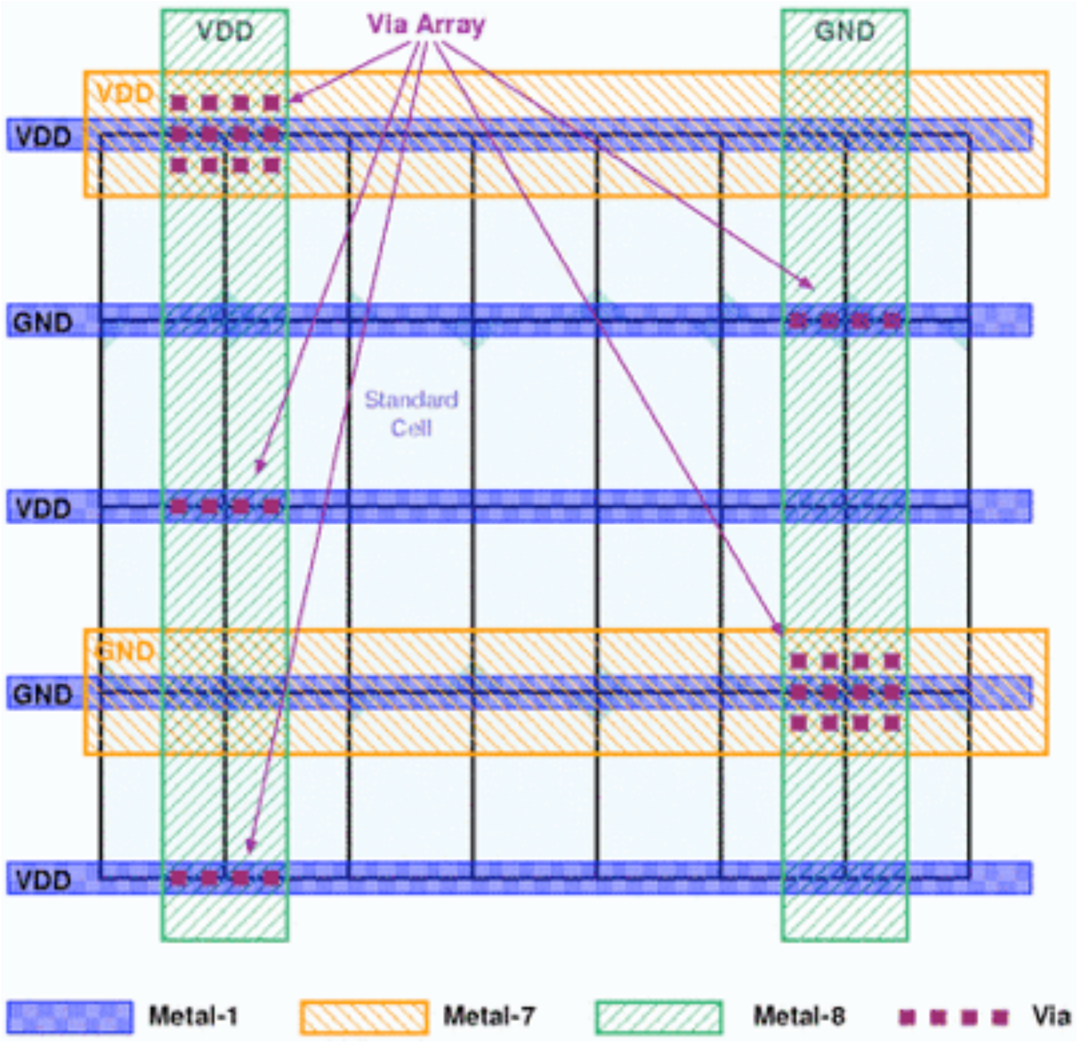


**Proximity** leads to stronger coupling through power lines

# Proximity leads again to coupling



**Proximity** leads to stronger coupling through power lines

Realistic assumption
**proximity leads to coupling**

# Does coupling affect the security of masked implementations?

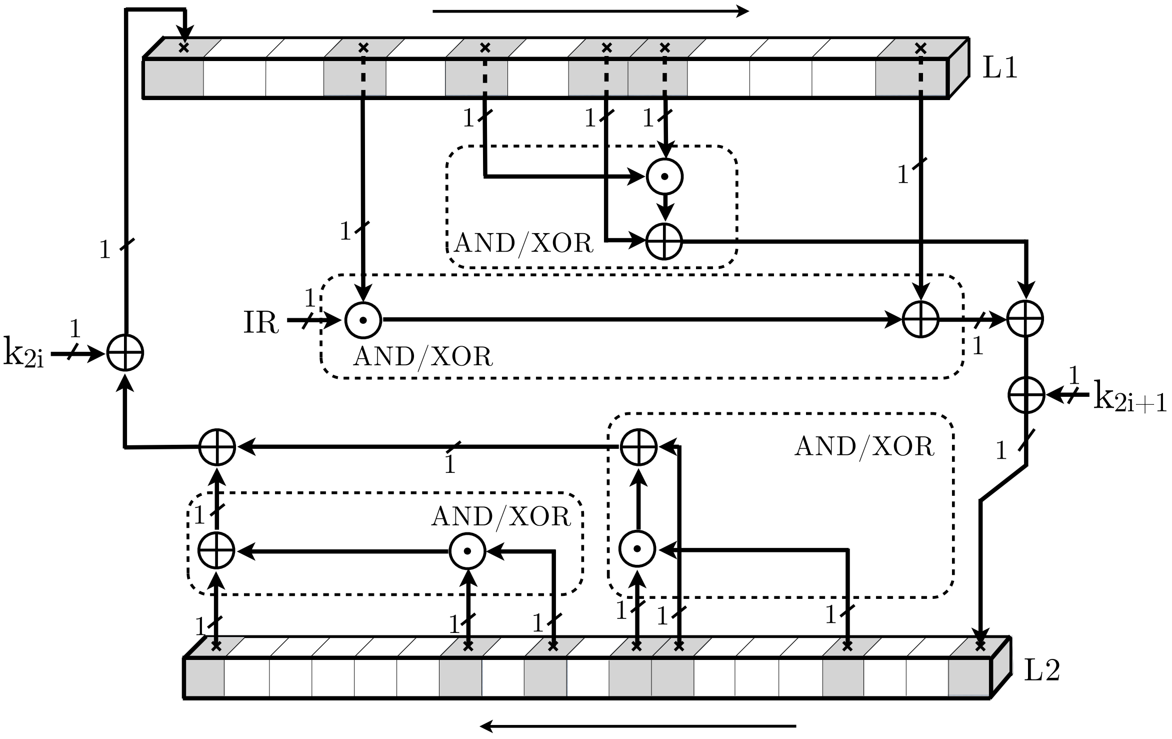
Masking
What can go wrong?

Sources of coupling
Proximity of shares

**Detecting coupling in practice**
Leakage is observable

Implications

# TI of KATAN-32 with 3 shares is used in our experiments



Low complexity of the nonlinear layer results in lower switching noise

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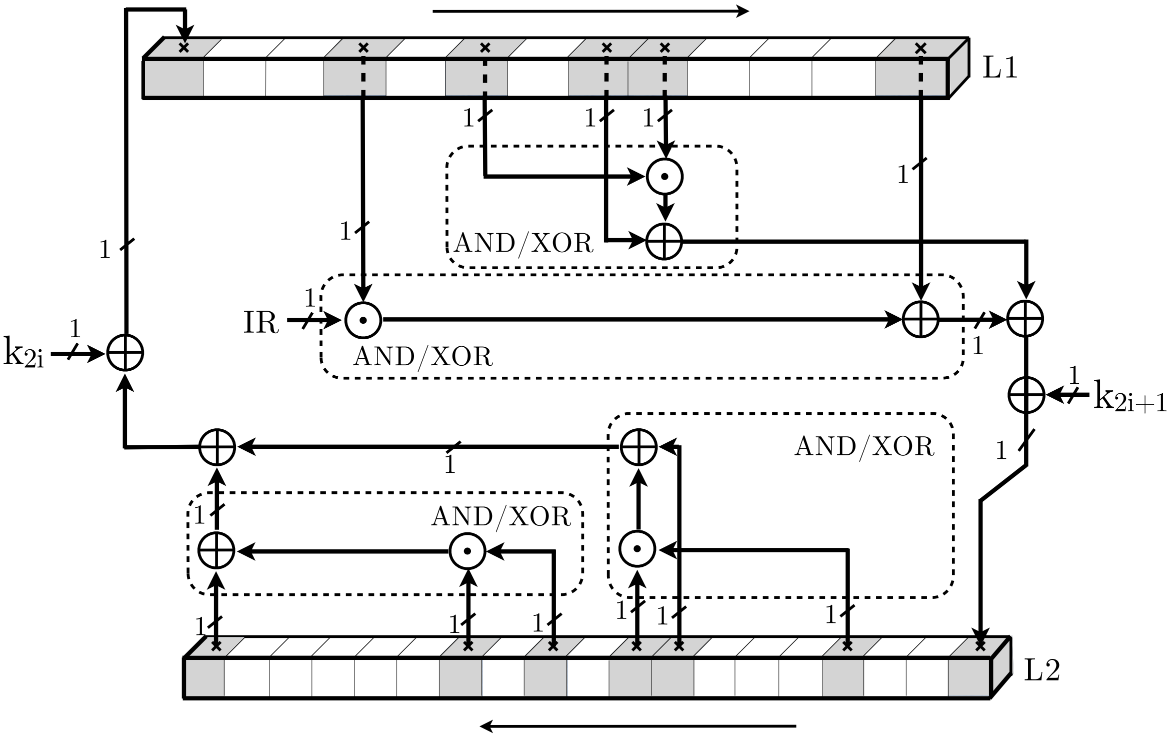
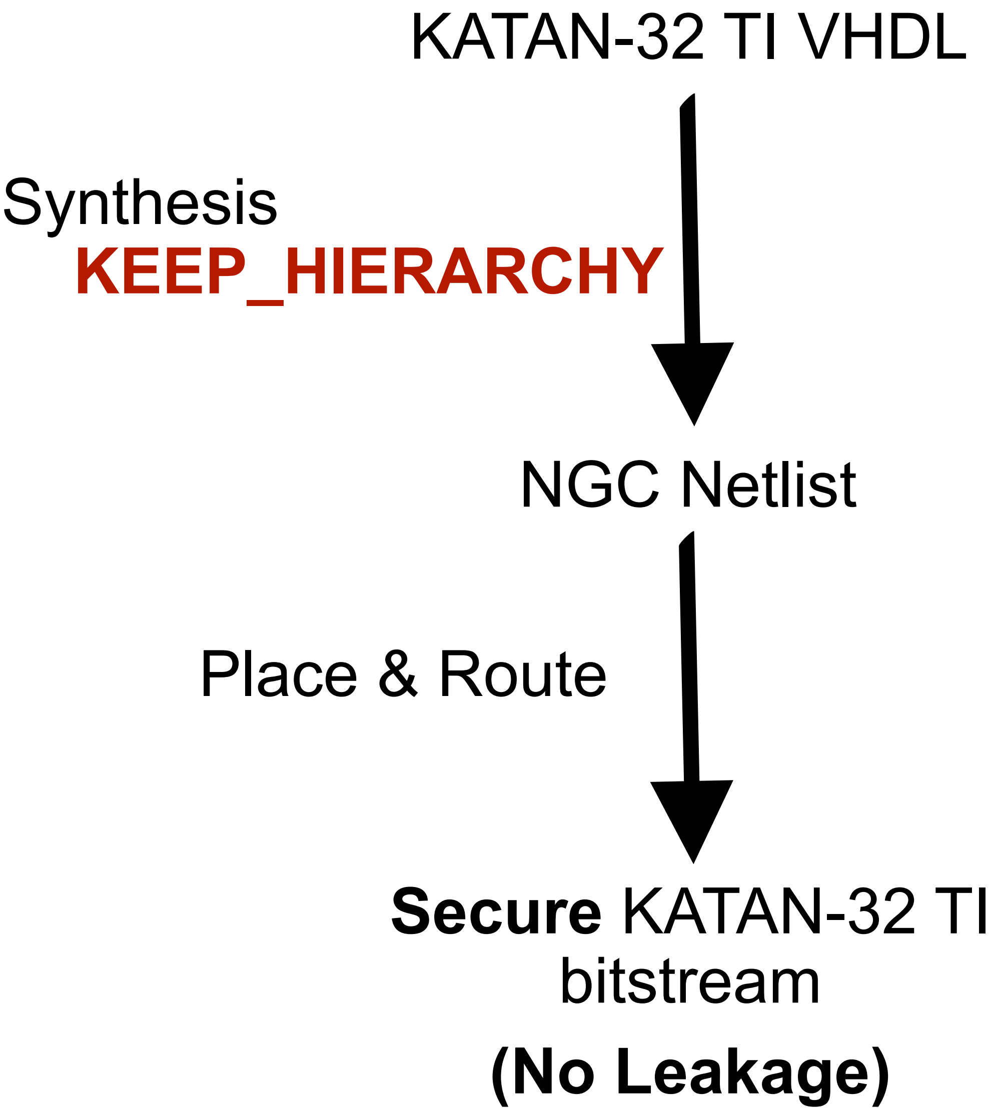


Low complexity of the nonlinear layer results in lower switching noise

and we expect this makes coupling easier to detect

# Avoiding optimizations over share boundaries is important for security



KATAN-32 TI VHDL

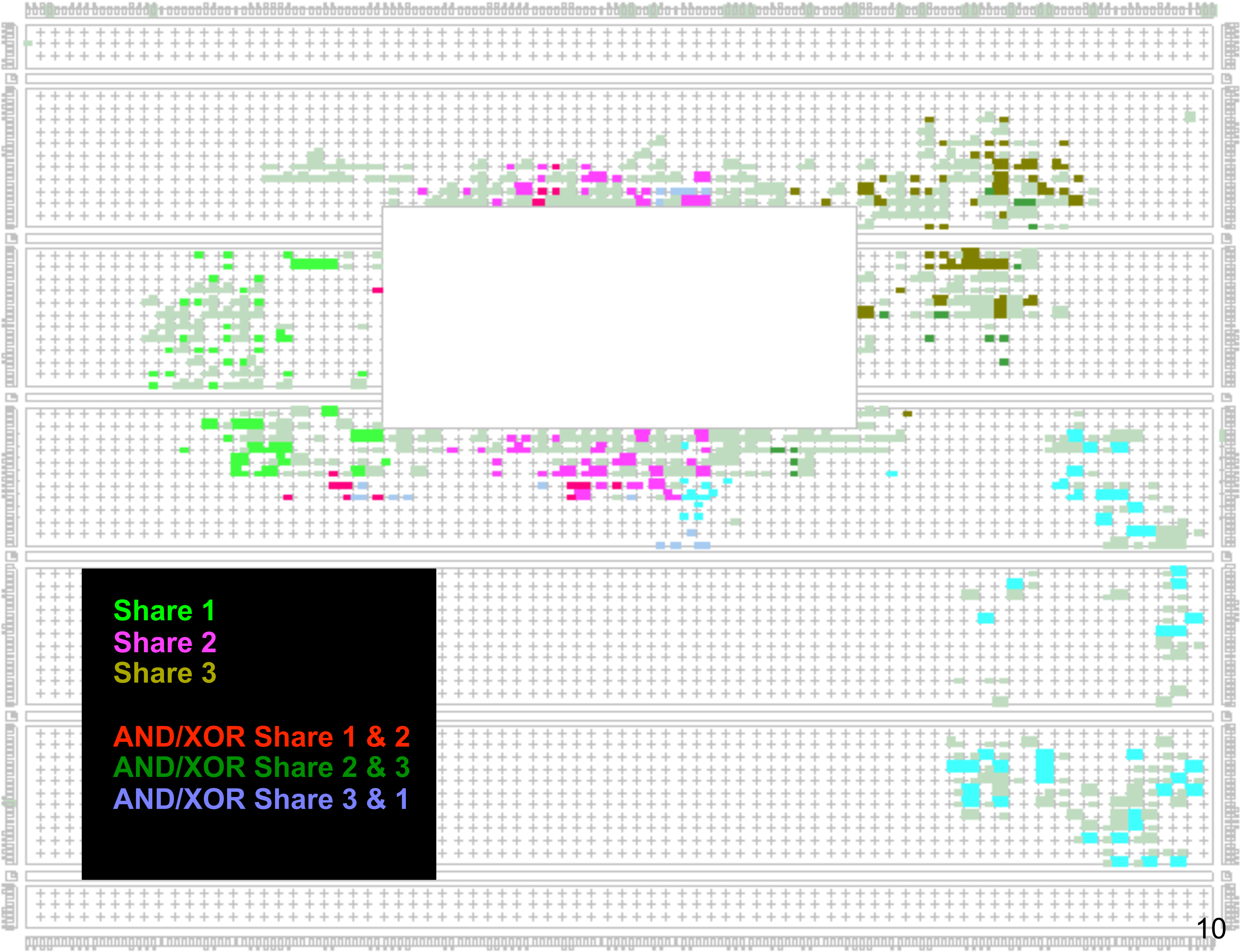
Synthesis
**KEEP_HIERARCHY**

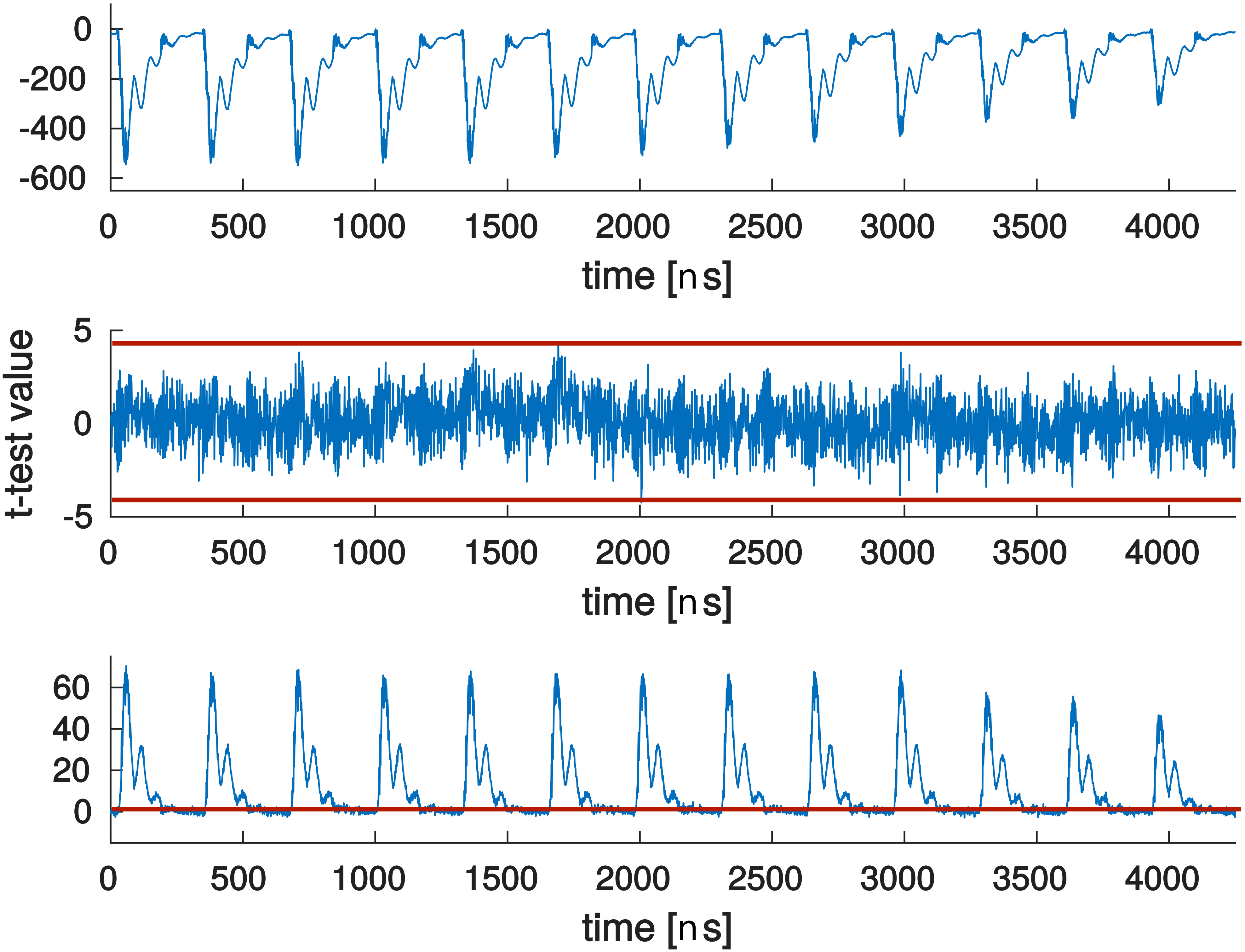
NGC Netlist

Place & Route

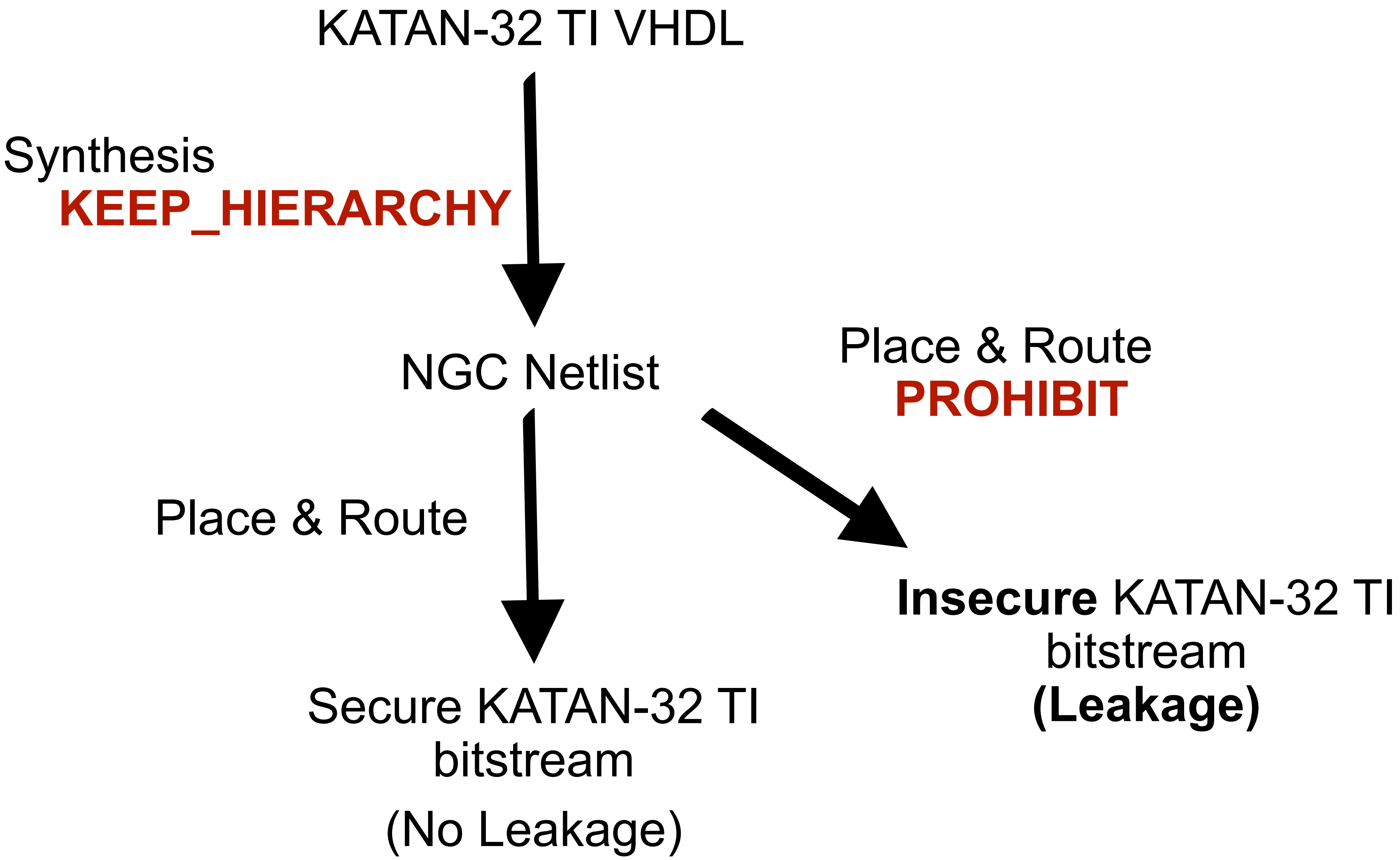
**Secure** KATAN-32 TI bitstream

**(No Leakage)**


Share 1
Share 2
Share 3
AND/XOR Share 1 & 2
AND/XOR Share 2 & 3
AND/XOR Share 3 & 1


0
-200
-400
-600
0
500
1000
1500
2000
2500
3000
3500
4000
time [ns]
t-test value
5
0
-5
0
500
1000
1500
2000
2500
3000
3500
4000
time [ns]
60
40
20
0
0
500
1000
1500
2000
2500
3000
3500
4000
time [ns]

# Bringing shares in close proximity is expected to lead to coupling



KATAN-32 TI VHDL

Synthesis
**KEEP_HIERARCHY**

NGC Netlist

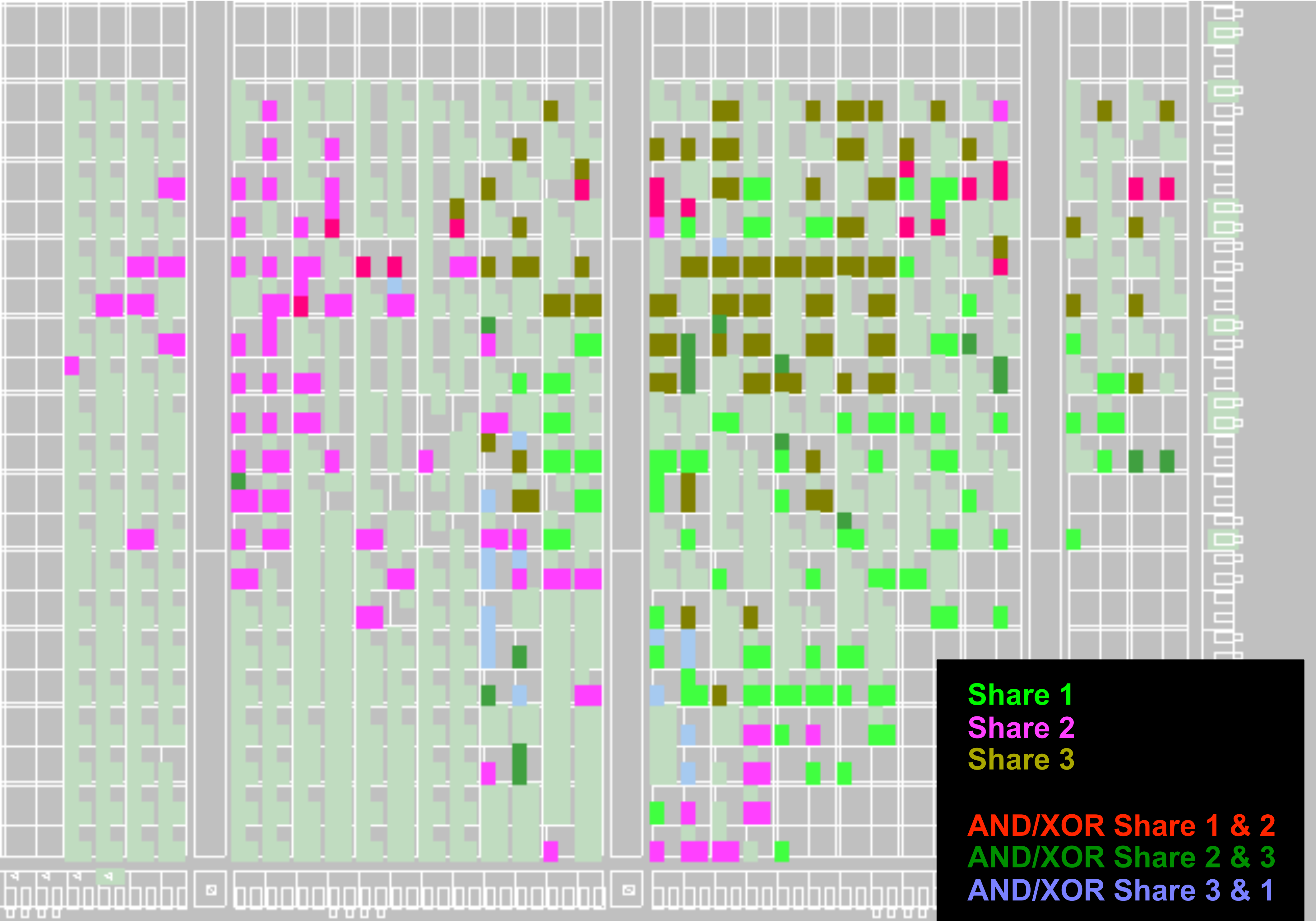
Place & Route

Place & Route
**PROHIBIT**

Secure KATAN-32 TI bitstream

(No Leakage)

**Insecure** KATAN-32 TI bitstream
**(Leakage)**



Share 1

Share 2

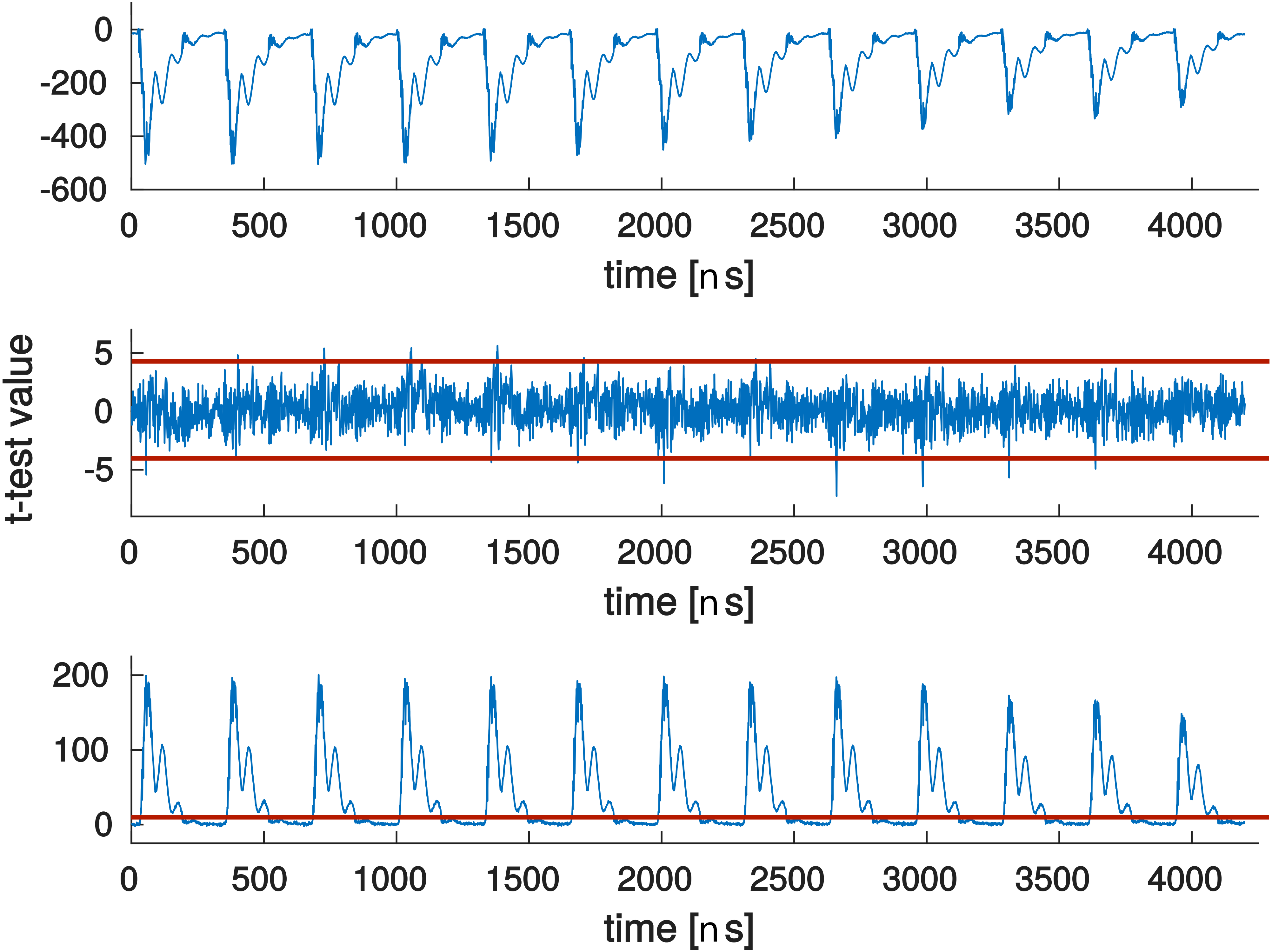
Share 3

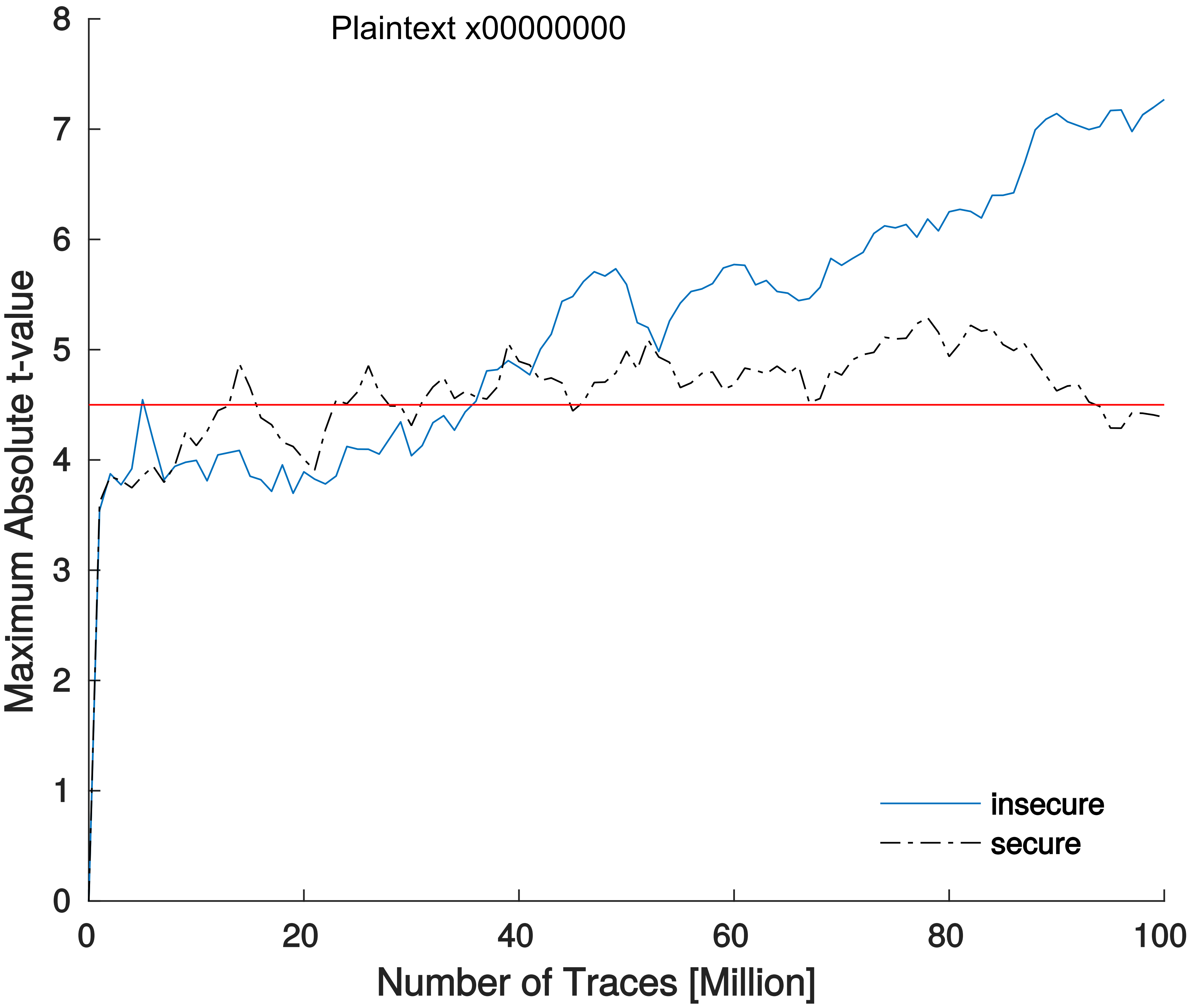
AND/XOR Share 1 & 2

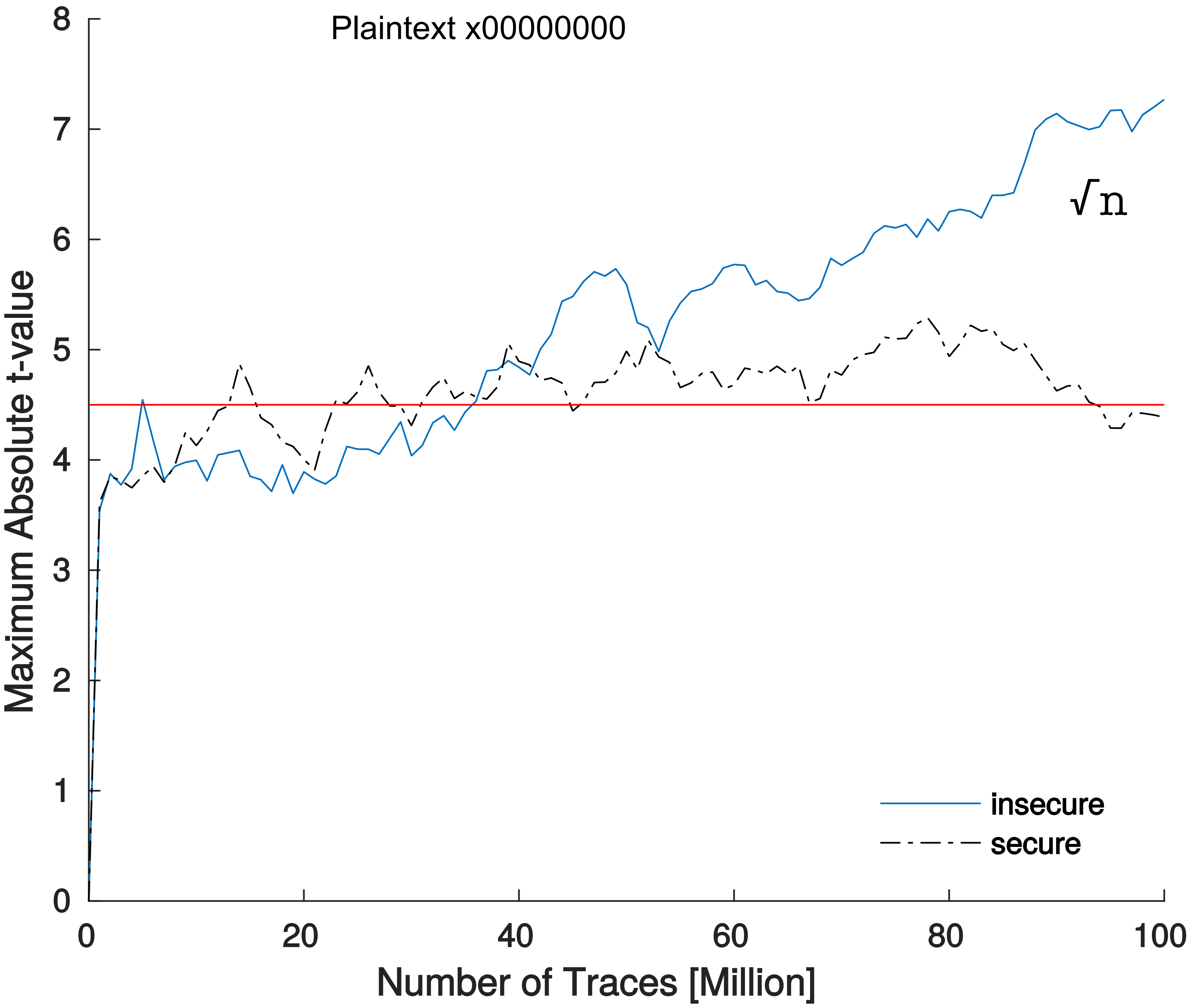
AND/XOR Share 2 & 3

AND/XOR Share 3 & 1

Shares are put in the lower right corner of the FPGA


0
-200
-400
-600
0
500
1000
1500
2000
2500
3000
3500
4000
time [n s]
t-test value
5
0
-5
0
500
1000
1500
2000
2500
3000
3500
4000
time [n s]
200
100
0
0
500
1000
1500
2000
2500
3000
3500
4000
time [n s]


Plaintext x00000000
Maximum Absolute t-value
0
1
2
3
4
5
6
7
8
0
20
40
60
80
100
Number of Traces [Million]
insecure
secure


Plaintext x00000000
√n
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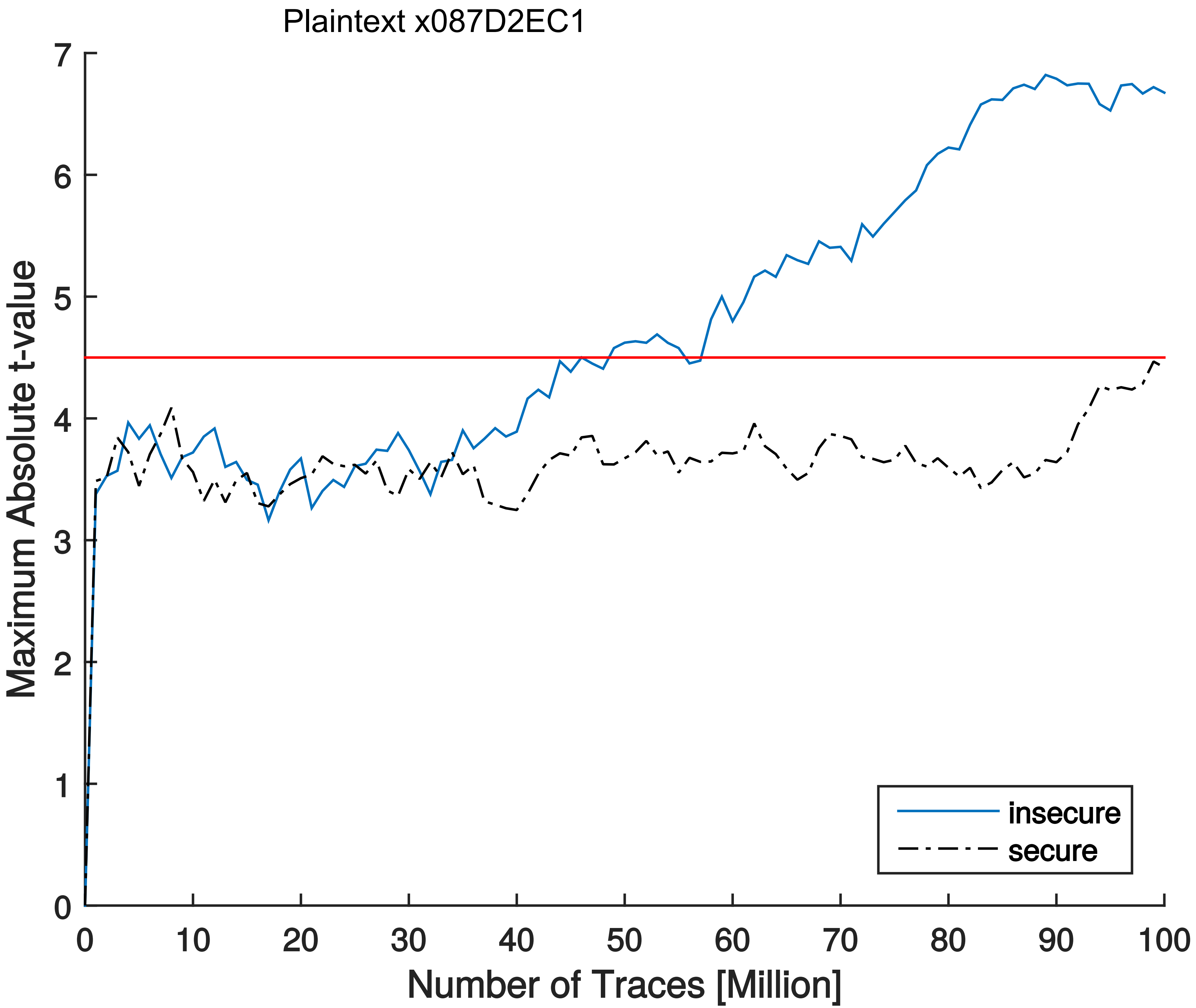
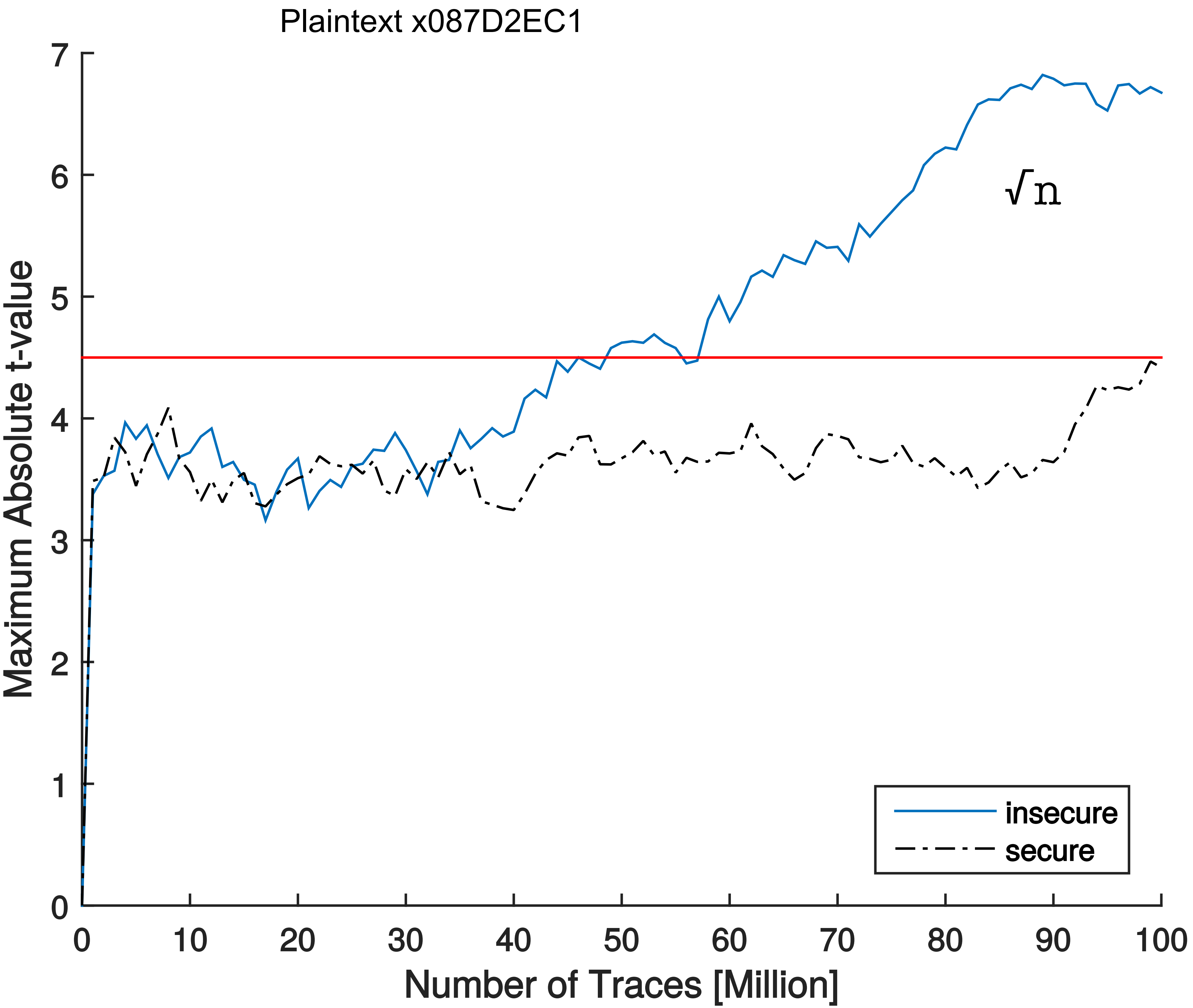

Plaintext x087D2EC1
Maximum Absolute t-value
0
1
2
3
4
5
6
7
Number of Traces [Million]
0
10
20
30
40
50
60
70
80
90
100
insecure
secure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40
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70
80
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√n
insecure
secure

# Does coupling affect the security of masked implementations?

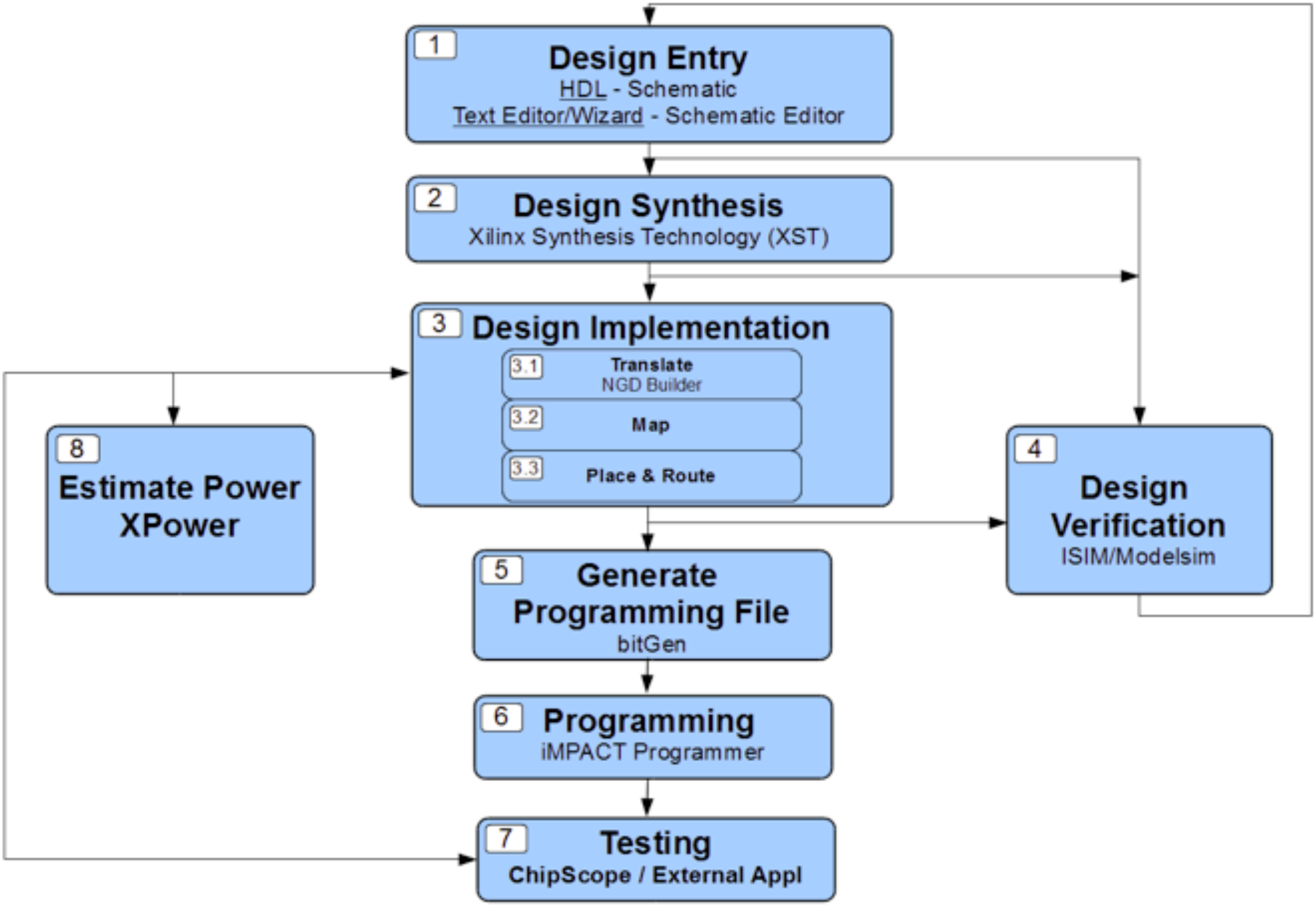
Masking
What can go wrong?

Sources of coupling
Proximity of shares

Detecting coupling in practice
Leakage is observable

**Implications**

# We control up to the placement stage
# Can we be sure?



1 Design Entry
HDL - Schematic
Text Editor/Wizard - Schematic Editor

2 Design Synthesis
Xilinx Synthesis Technology (XST)

3 Design Implementation
3.1 Translate
NGD Builder
3.2 Map
3.3 Place & Route

4 Design Verification
ISIM/Modelsim

5 Generate Programming File
bitGen

6 Programming
iMPACT Programmer

7 Testing
ChipScope / External Appl

8 Estimate Power
XPower

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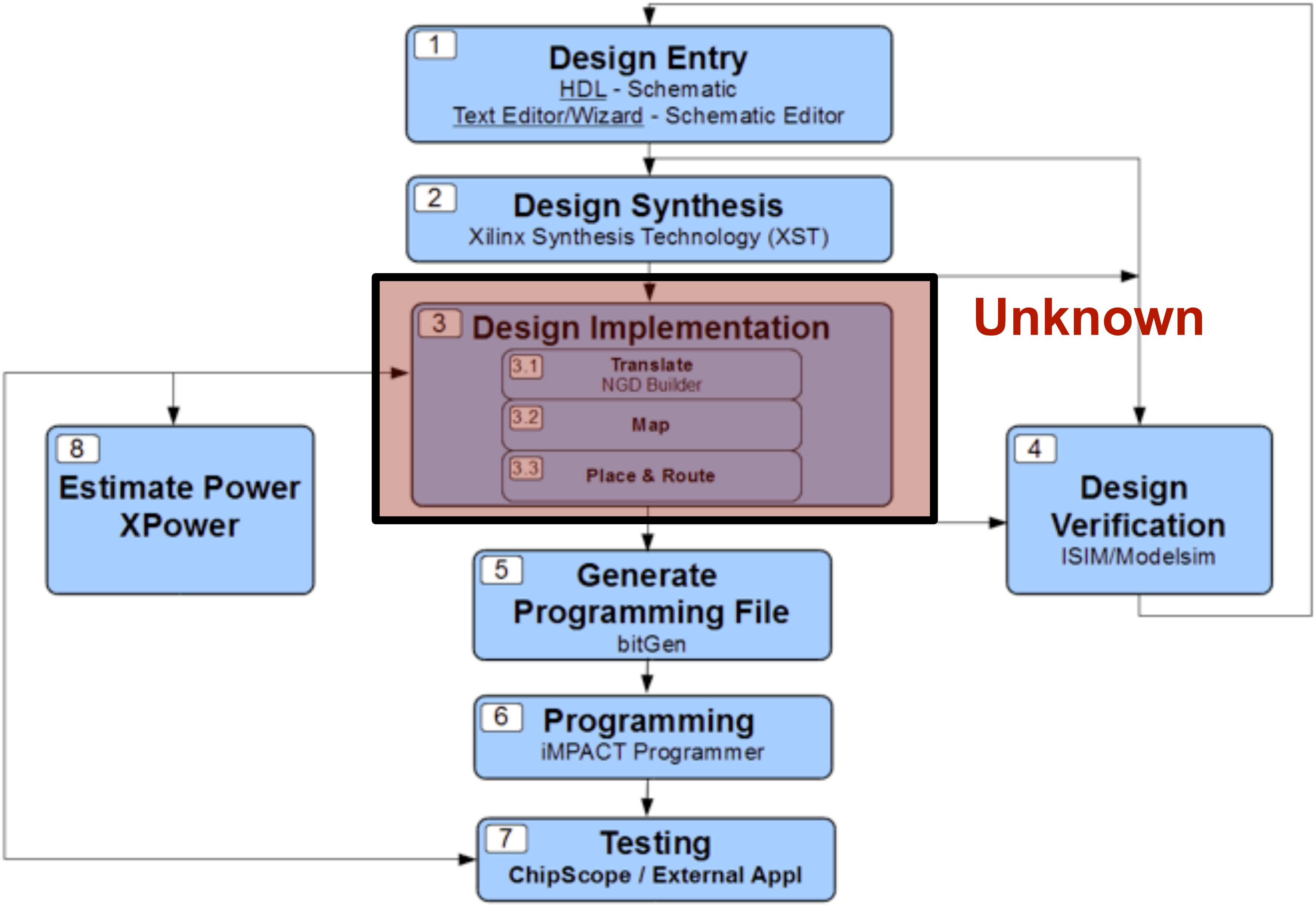
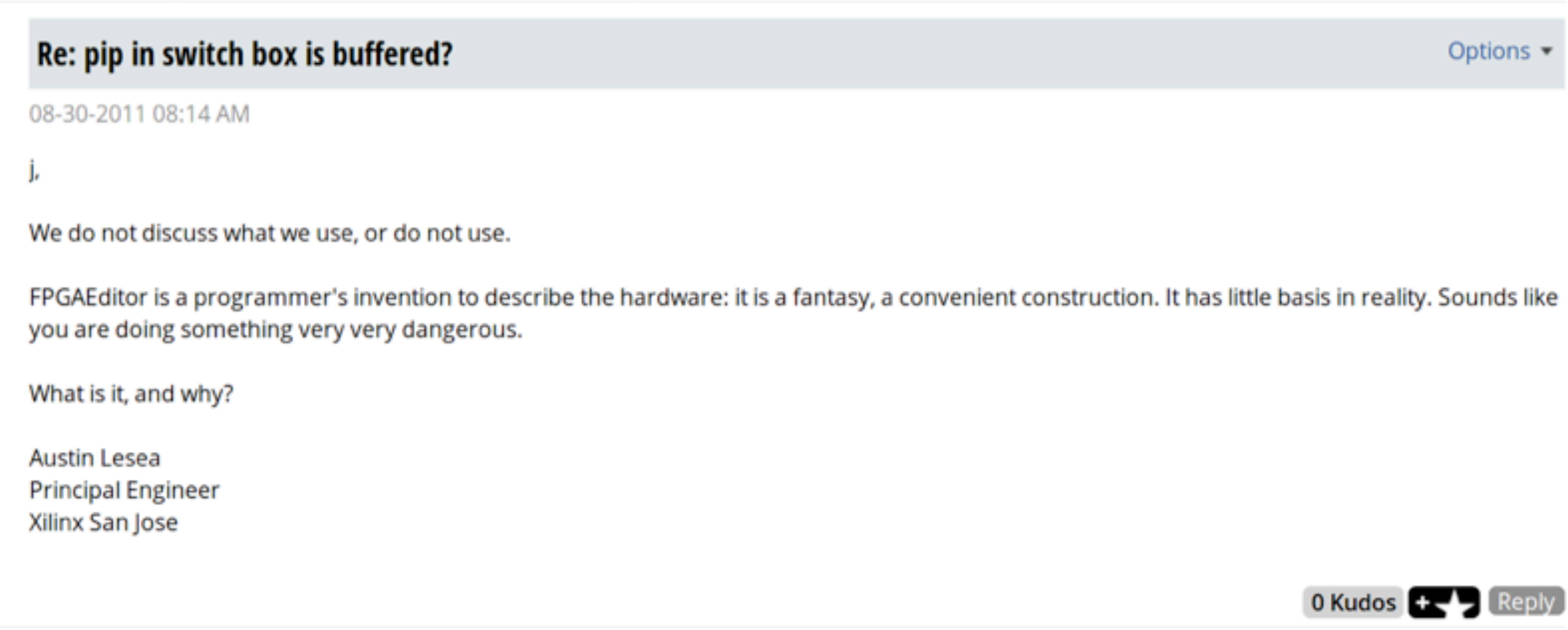
# Can we be sure?



# The FPGA is a black box
# Can we be sure?



**Re: pip in switch box is buffered?**

08-30-2011 08:14 AM

j,

We do not discuss what we use, or do not use.

FPGAEditor is a programmer's invention to describe the hardware: it is a fantasy, a convenient construction. It has little basis in reality. Sounds like you are doing something very very dangerous.

What is it, and why?

Austin Lesea
Principal Engineer
Xilinx San Jose

# Coupling becomes more prominent in smaller technology nodes

90nm
SASEBO-G

65nm
SASEBO-GII

45nm
SAKURA-G

28nm
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2004

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2004

What can we expect for modern and future platforms?

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- Technology? ASIC vs FPGA?
- How to implement masking schemes securely?

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- Technology? ASIC vs FPGA?
- How to implement masking schemes securely?
- **Is key retrieval possible?**

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